the input signals in parallel from the input circuitry to the output circuitry.

104.(New) The circuitry defined in claim 103 wherein the factor is programmable to equal the programmable number.

105.(New) The circuitry defined in claim 102 wherein the input circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

106.(New) The circuitry defined in claim 105 wherein the register stages store the input signals in parallel.

107.(New) The circuitry defined in claim 106 wherein the register stages further output in parallel to the output circuitry information indicative of the input signals.

108.(New) The circuitry defined in claim 102 wherein the output circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

109.(New) The circuitry defined in claim 108 wherein the register stages store in parallel information from the input circuitry indicative of the input signals.

110.(New) The circuitry defined in claim 109 wherein the output circuitry further outputs information from the registers in a predetermined series one after another.

111.(New) A programmable system comprising:

programmable serializer circuitry as defined in claim 102; and

programmable logic circuitry for supplying the input signals.

112. (New) Programmable deserializer circuitry comprising:

input circuitry that receives an input signal serially indicative of plural bits of information one after another and stores a programmable number of successive ones of those bits; and

output circuitry that produces a plurality of output signals in parallel, each of the output signals being indicative of a respective one of the bits stored by the input circuitry.

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113. (New) The circuitry defined in claim 112 wherein the input signal is synchronized with a first clock signal having a first clock rate, and wherein the circuitry further comprises:

clock rate divider circuitry that divides the clock rate by a programmable factor to produce a second clock signal for timing the passage of information indicative of the bits stored by the input circuitry in parallel from the input circuitry to the output circuitry.

114. (New) The circuitry defined in claim 113 wherein the factor is programmable to equal the programmable number.

115. (New) The circuitry defined in claim 112 wherein the input circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

116. (New) The circuitry defined in claim 115 wherein each of the register stages stores one of the bits.

117.(New) The circuitry defined in claim 116 wherein the register stages further output in parallel to the output circuitry information indicative of the bits stored in the register stages.

118.(New) The circuitry defined in claim 112 wherein the output circuitry comprises a predetermined plural quantity of register stages, and wherein the number is programmable to any integer value up to and including the plural quantity.

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119.(New) The circuitry defined in claim 118 wherein the register stages store in parallel information from the input circuitry indicative of the bits stored by the input circuitry.

120.(New) The circuitry defined in claim 119 wherein the output circuitry further outputs information from the registers in parallel.

121.(New) A programmable system comprising:

programmable deserializer circuitry as defined in claim 112; and

programmable logic circuitry for receiving the output signals.